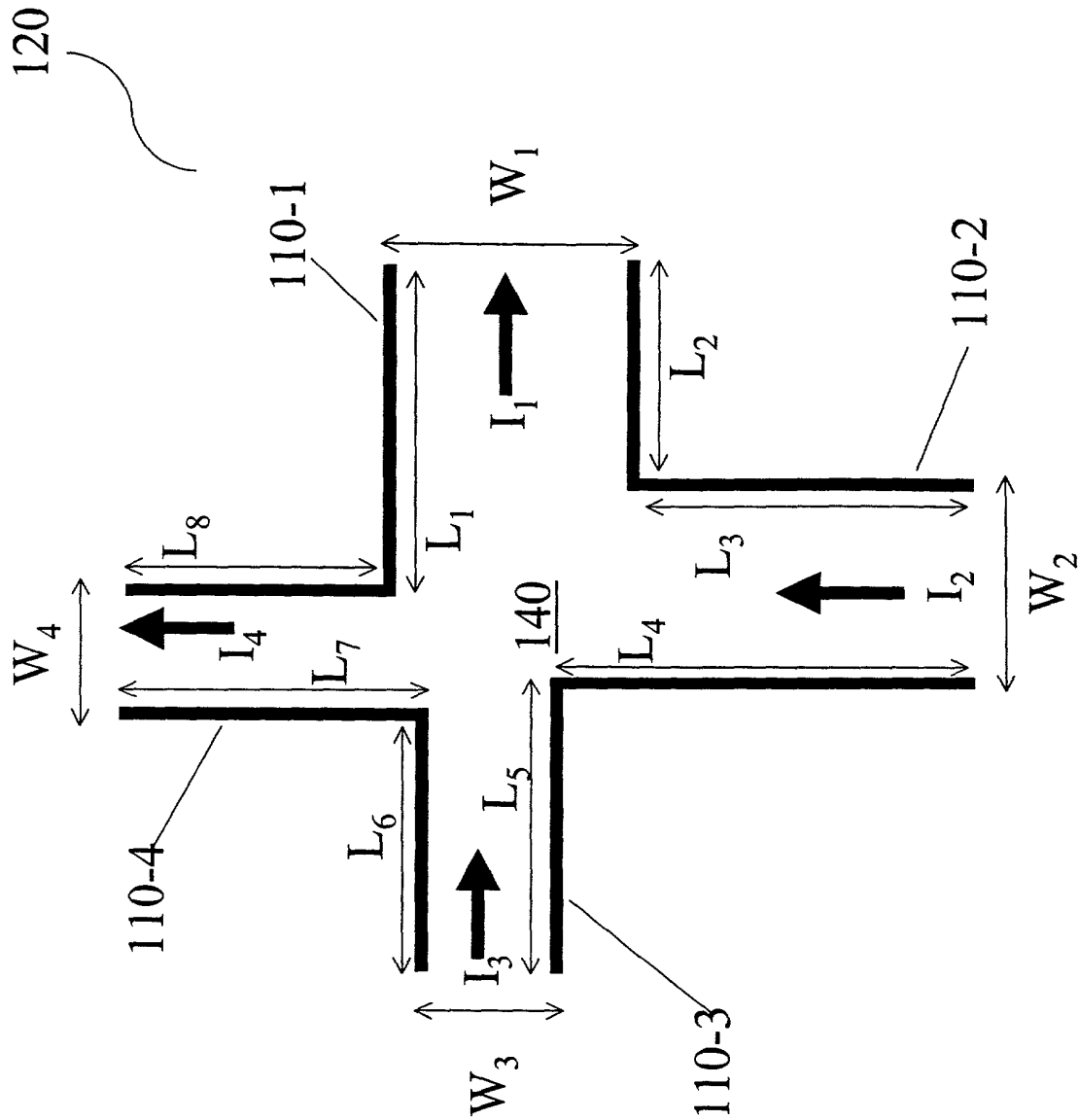


Figure 1A



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Figure 1B

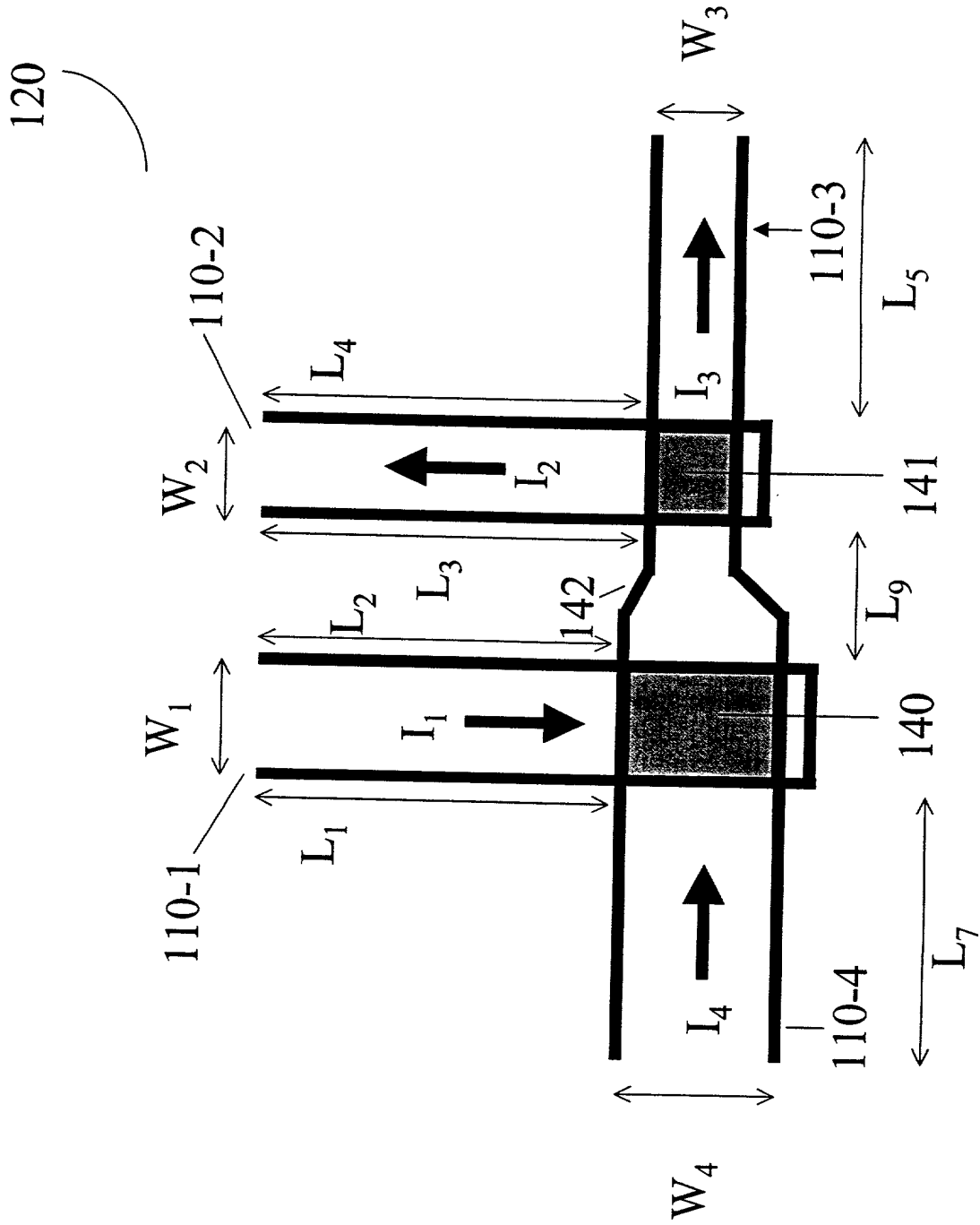


Figure 1C

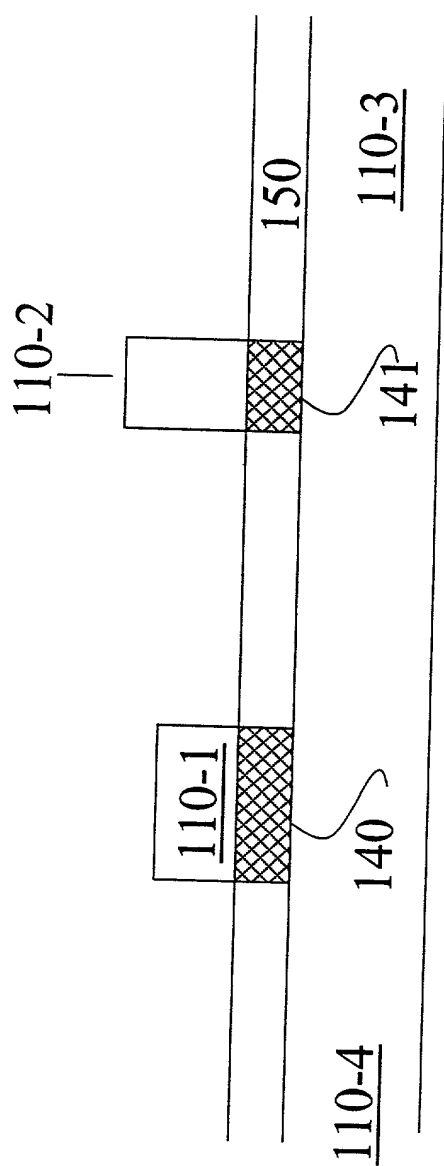


Figure 1D

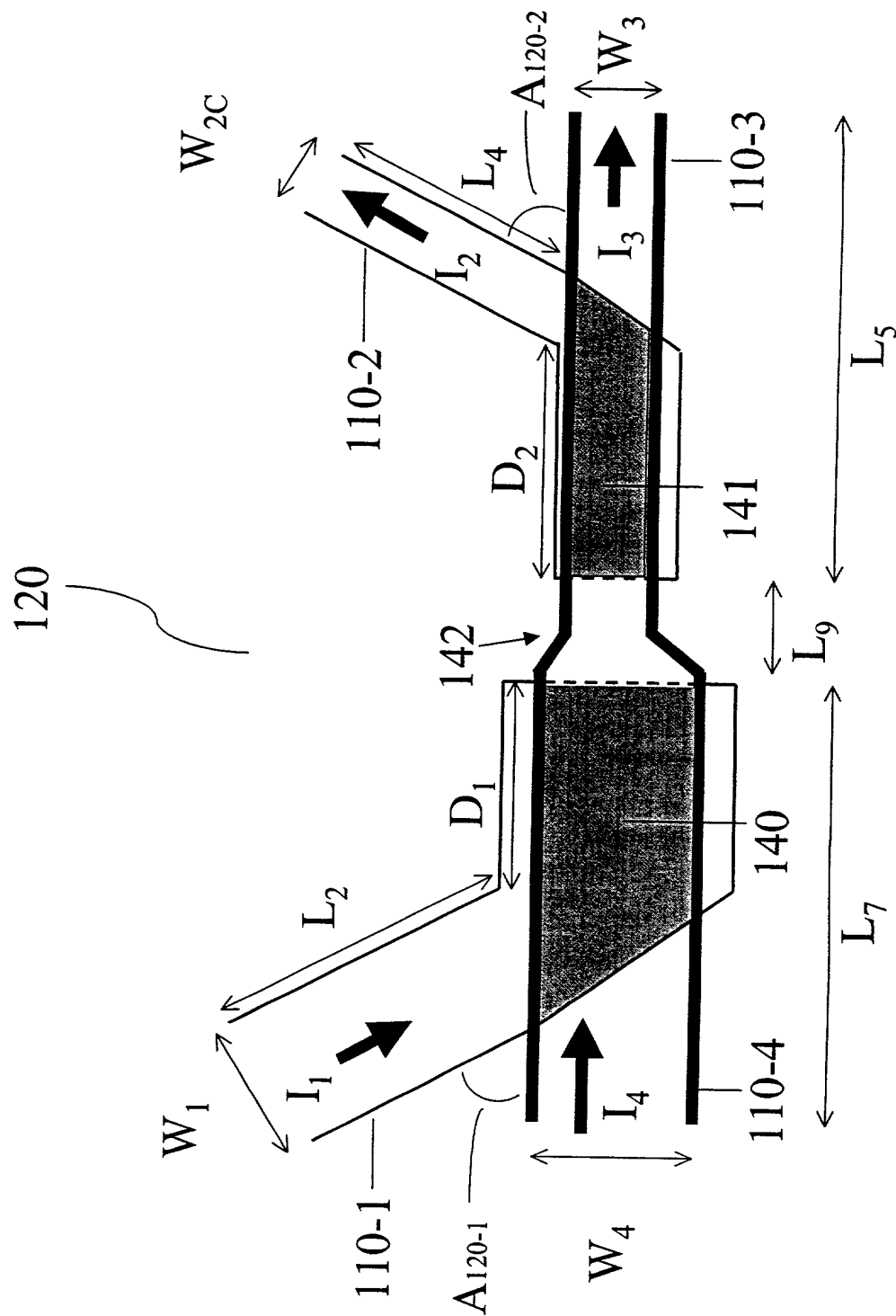


Figure 1F

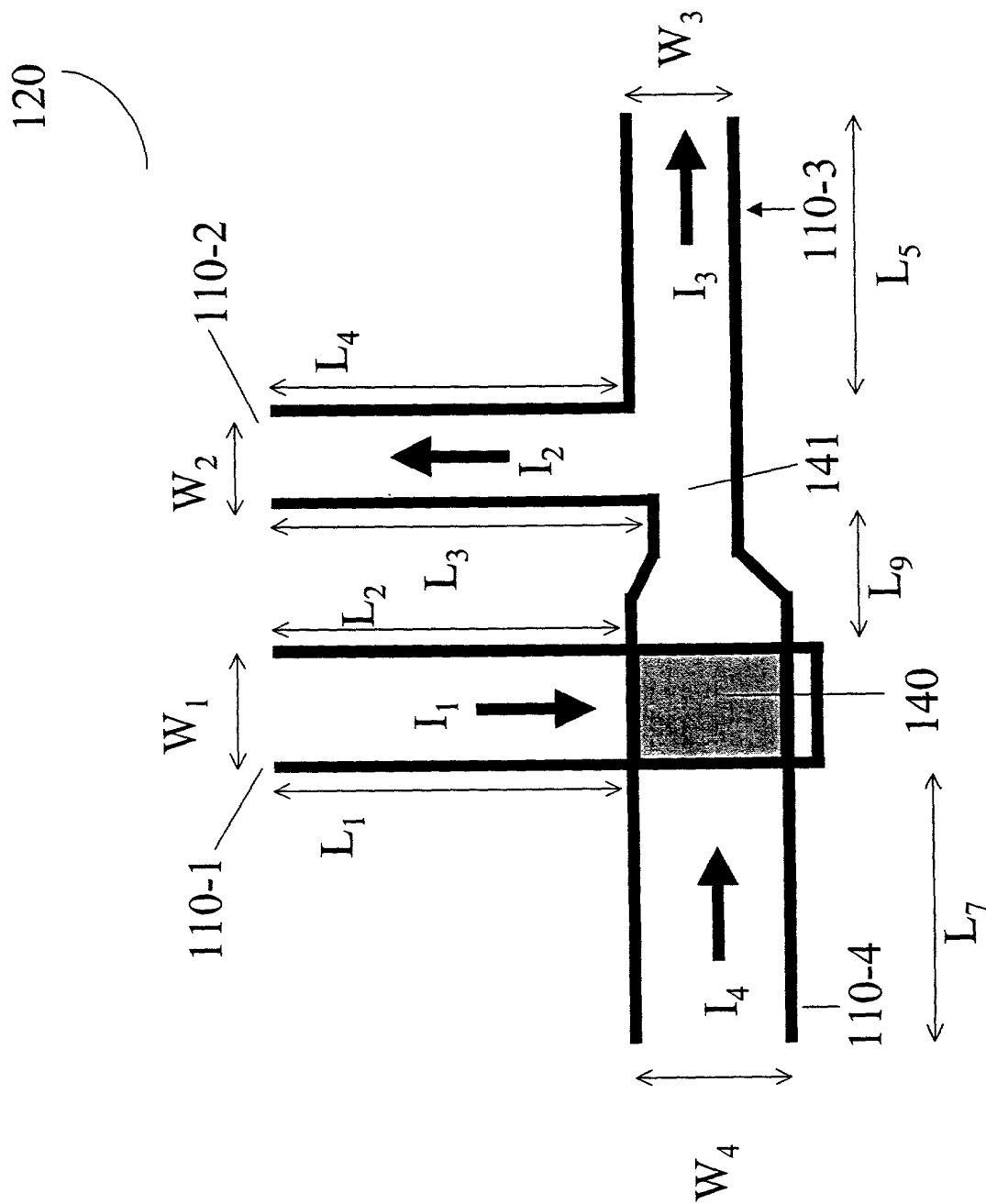


Figure 1G

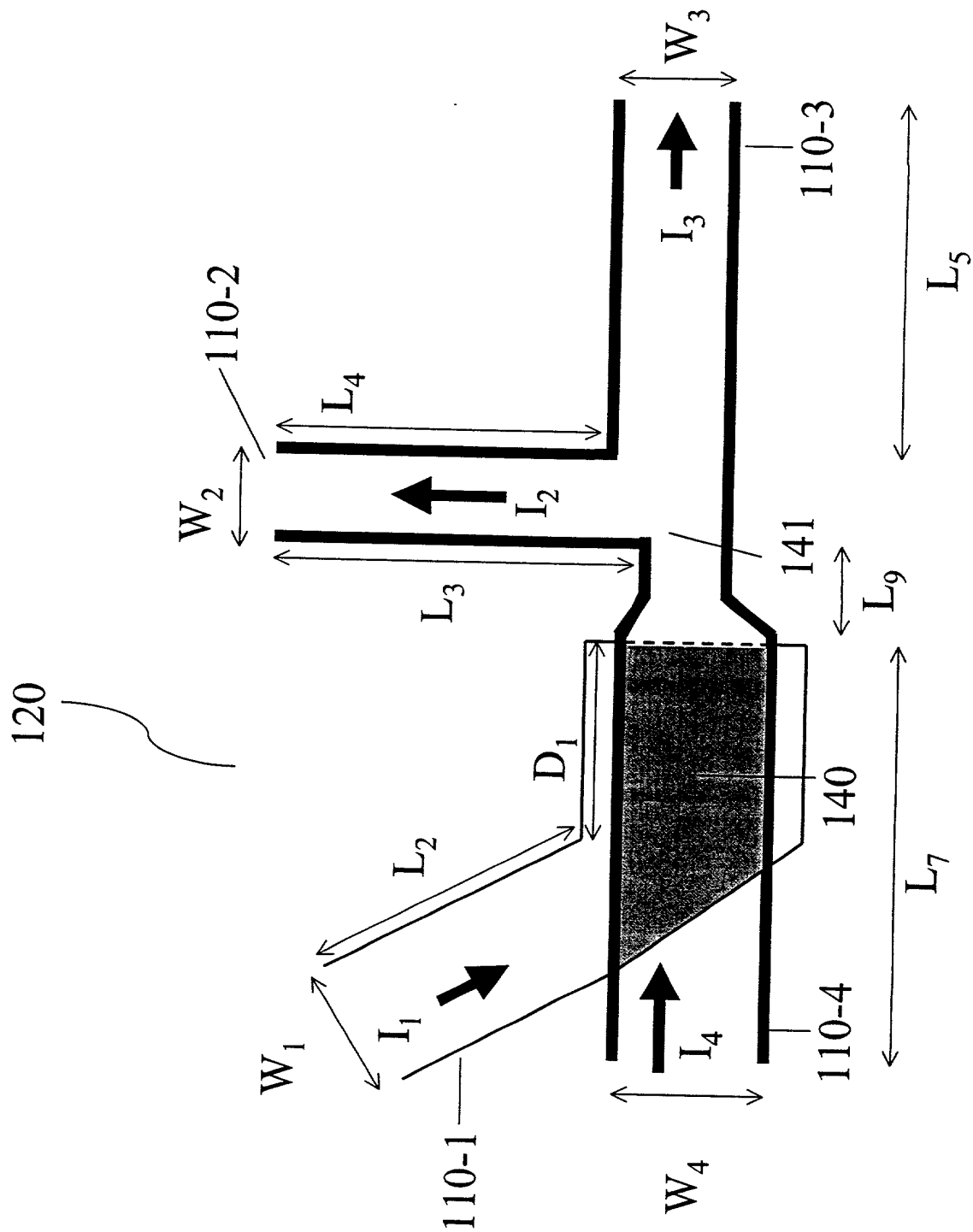


FIGURE 1H

Figure 1H

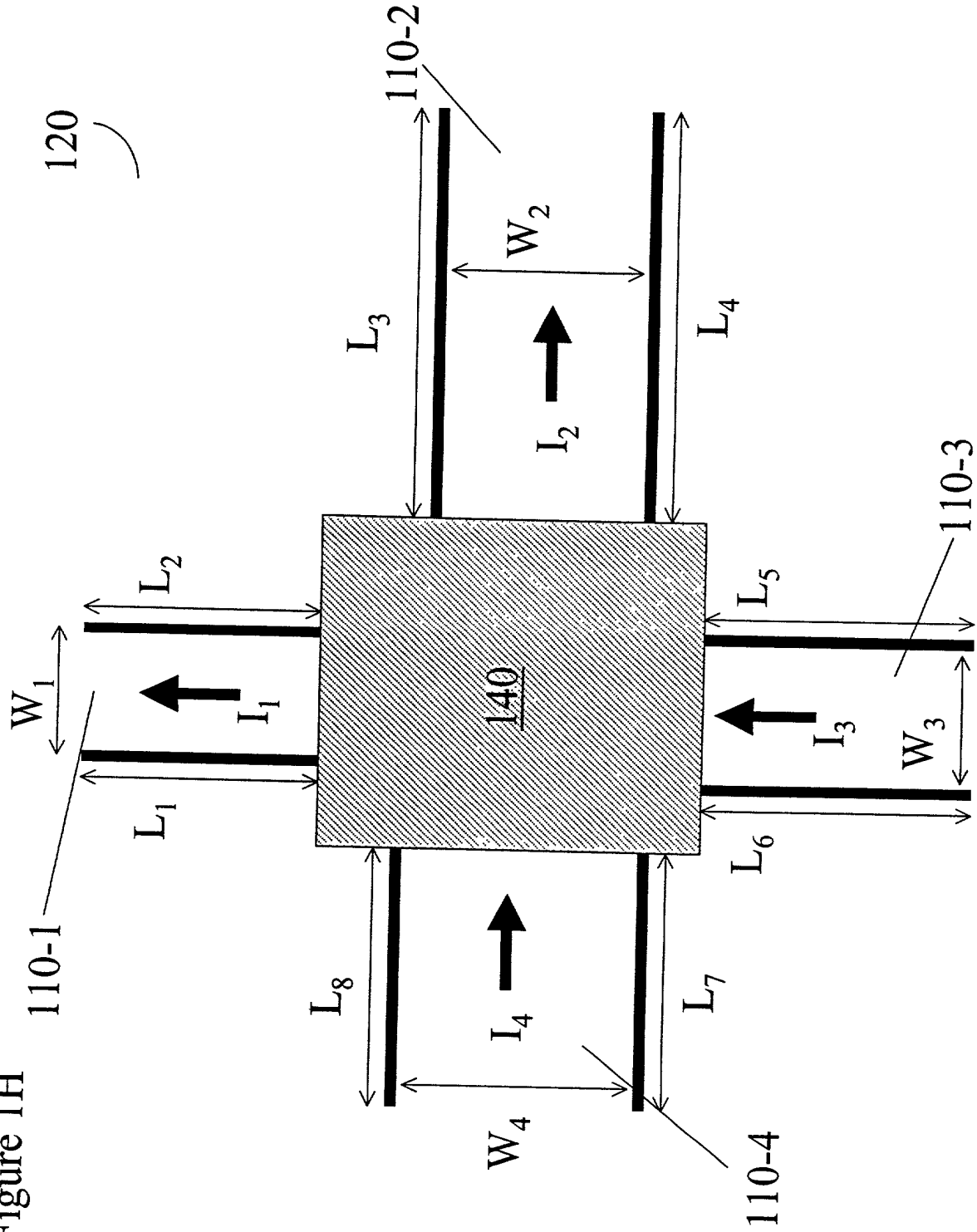
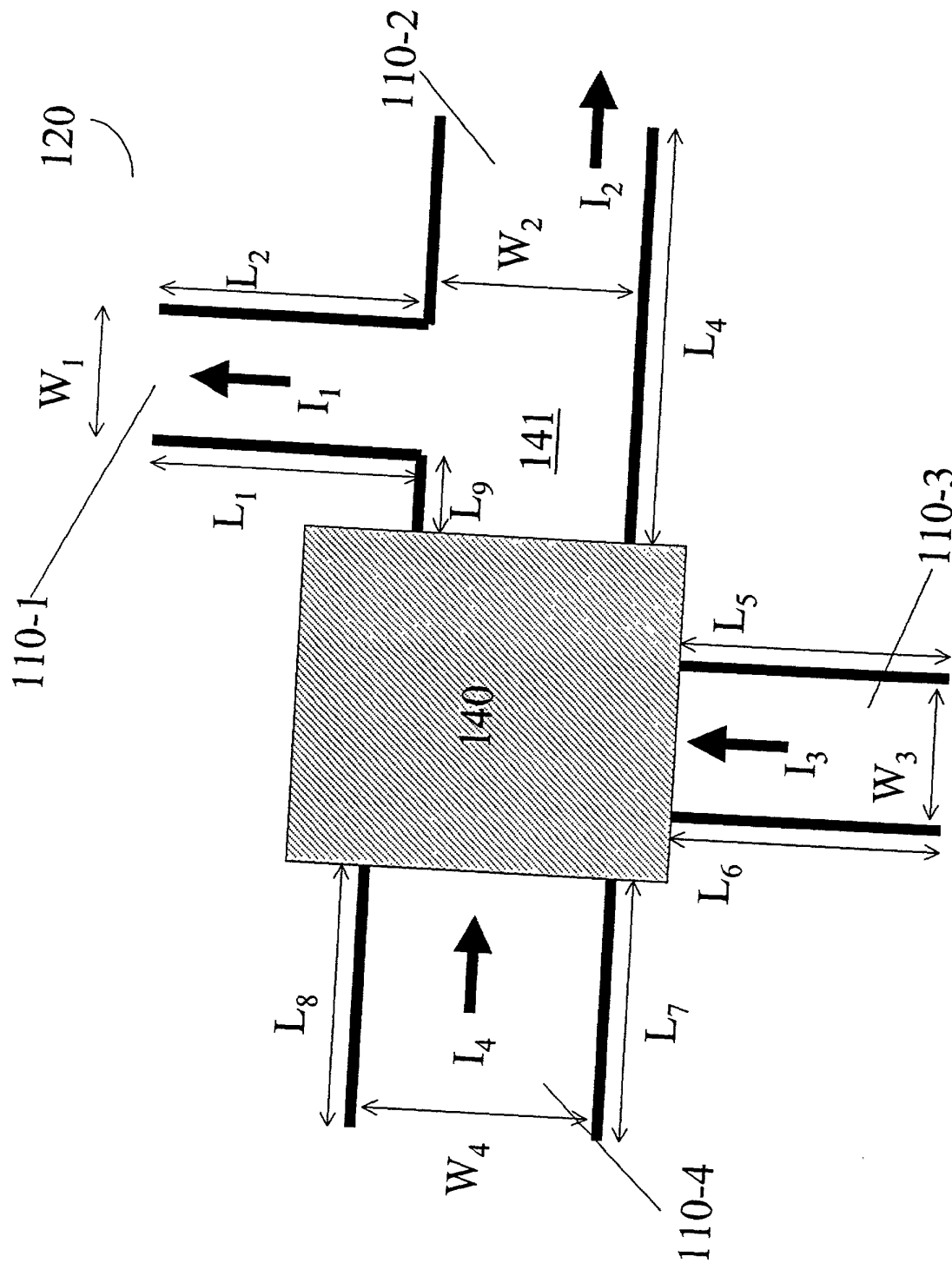
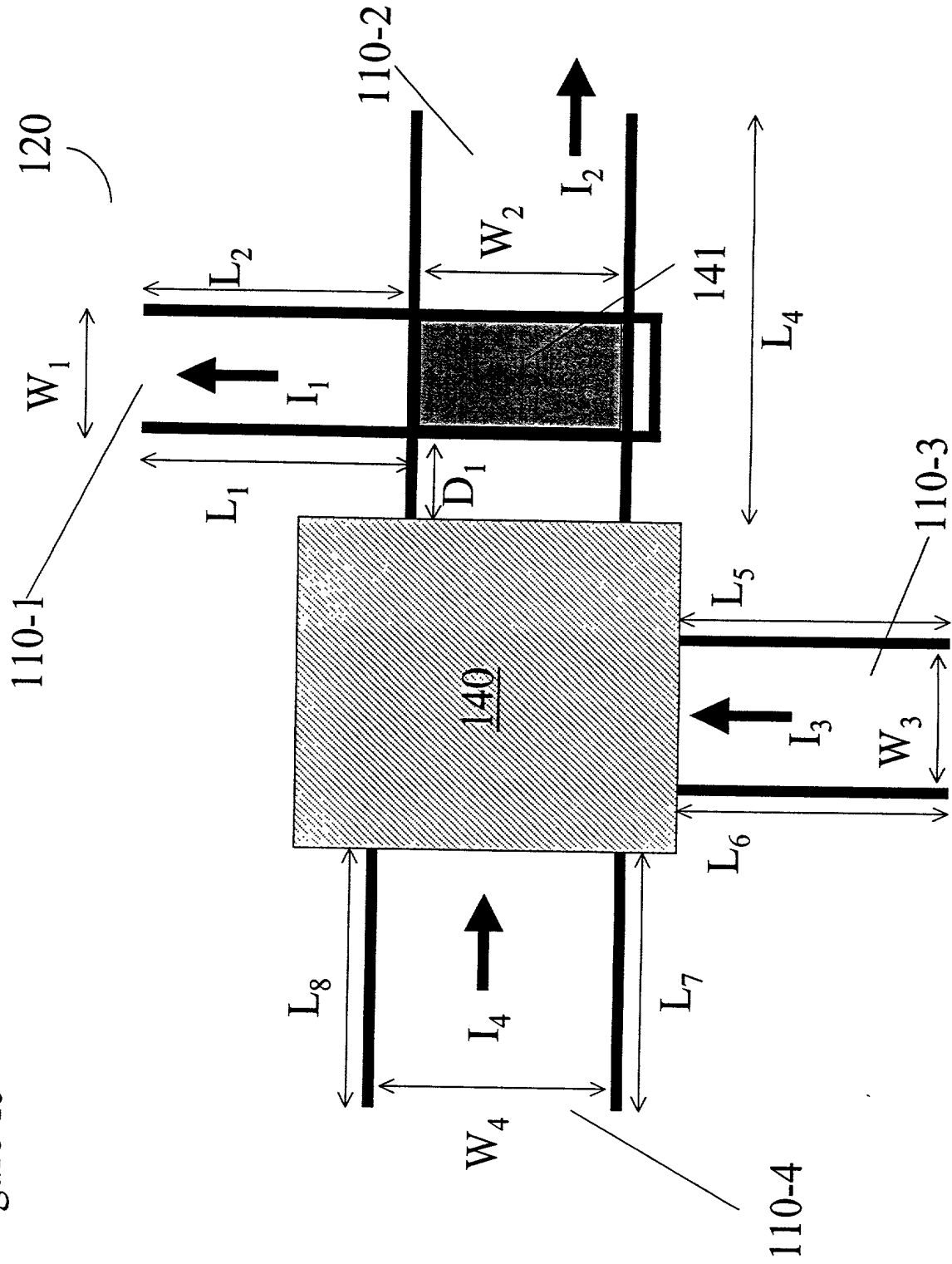


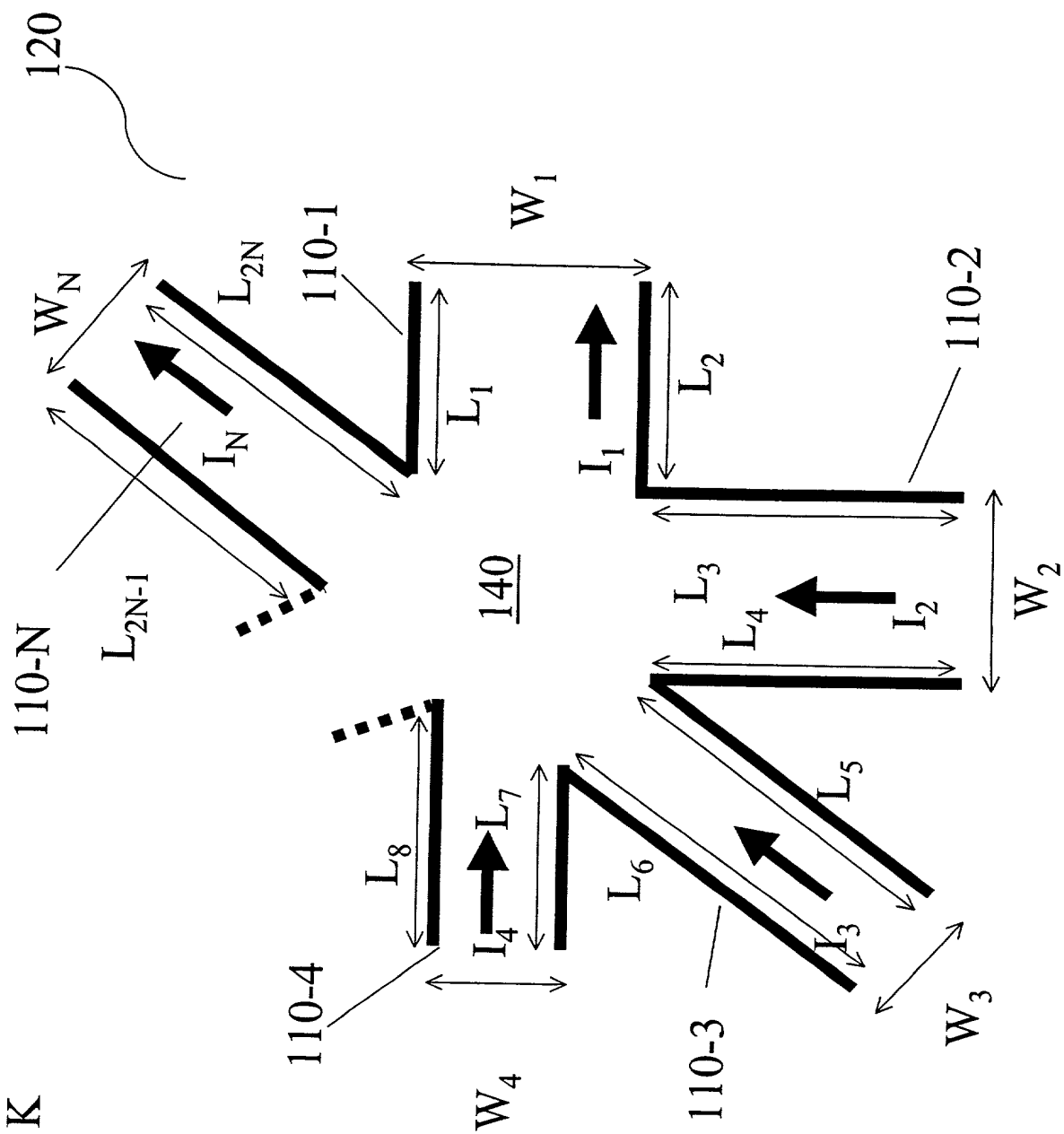
Figure 1I

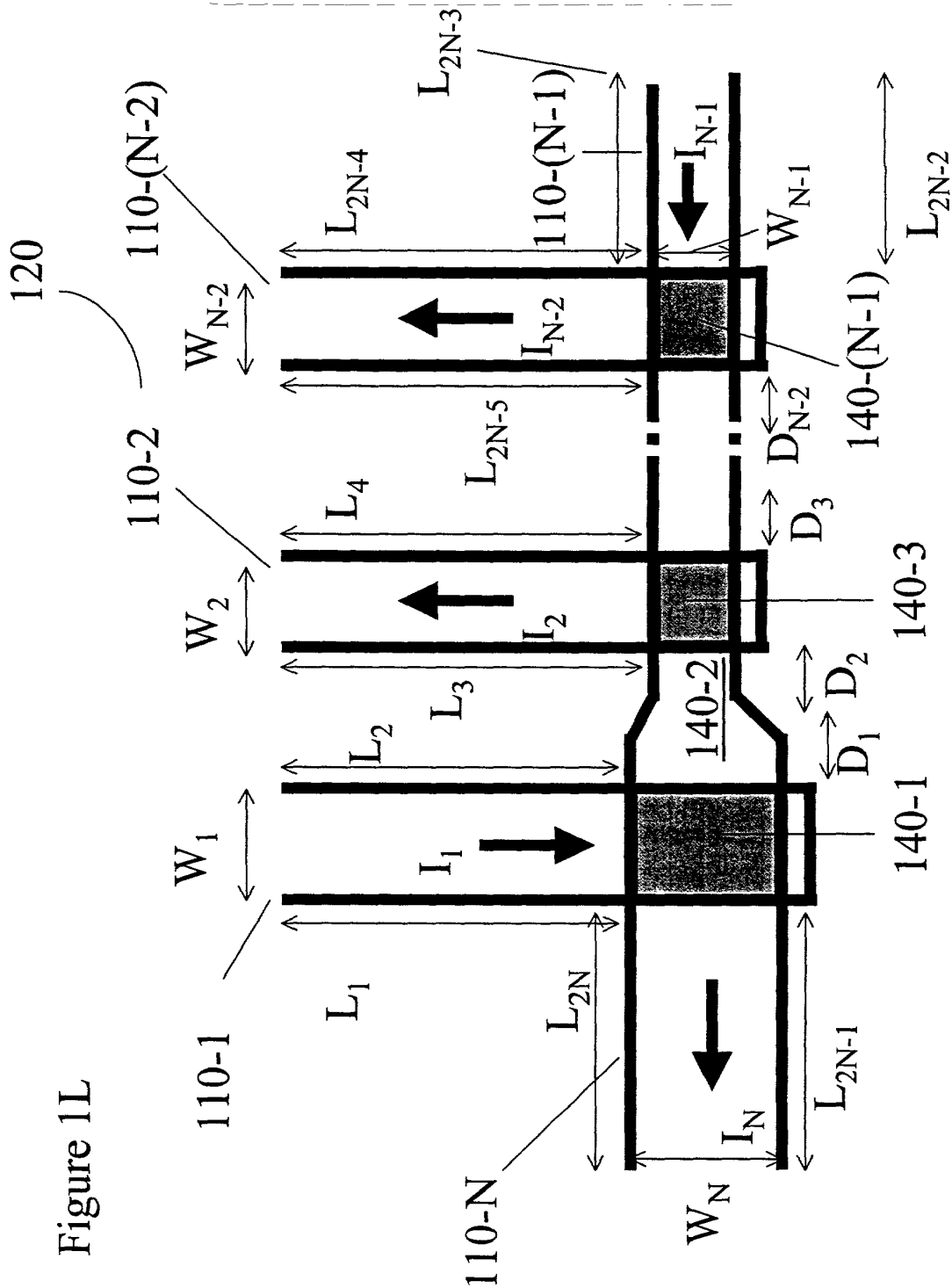


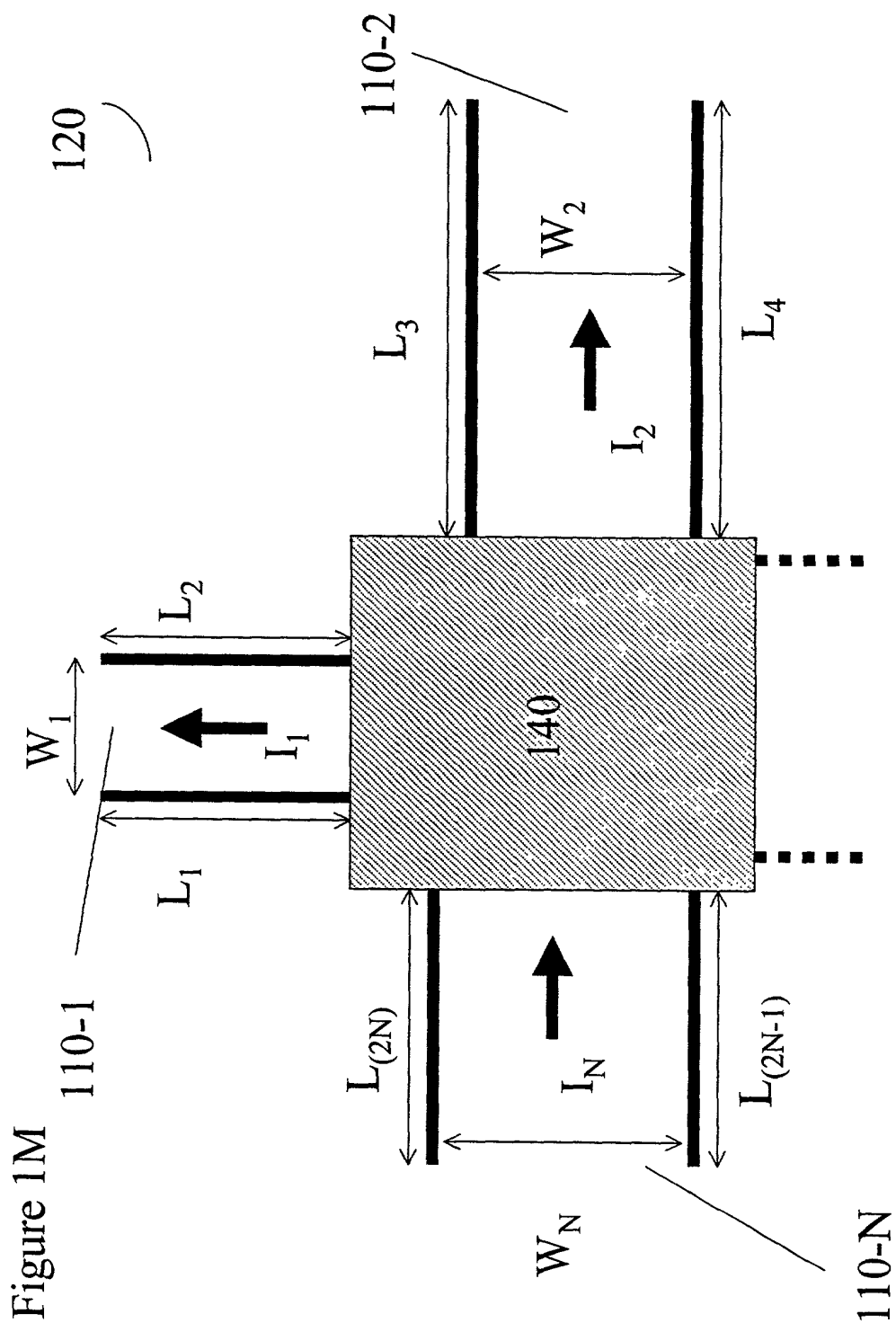
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Figure 1J



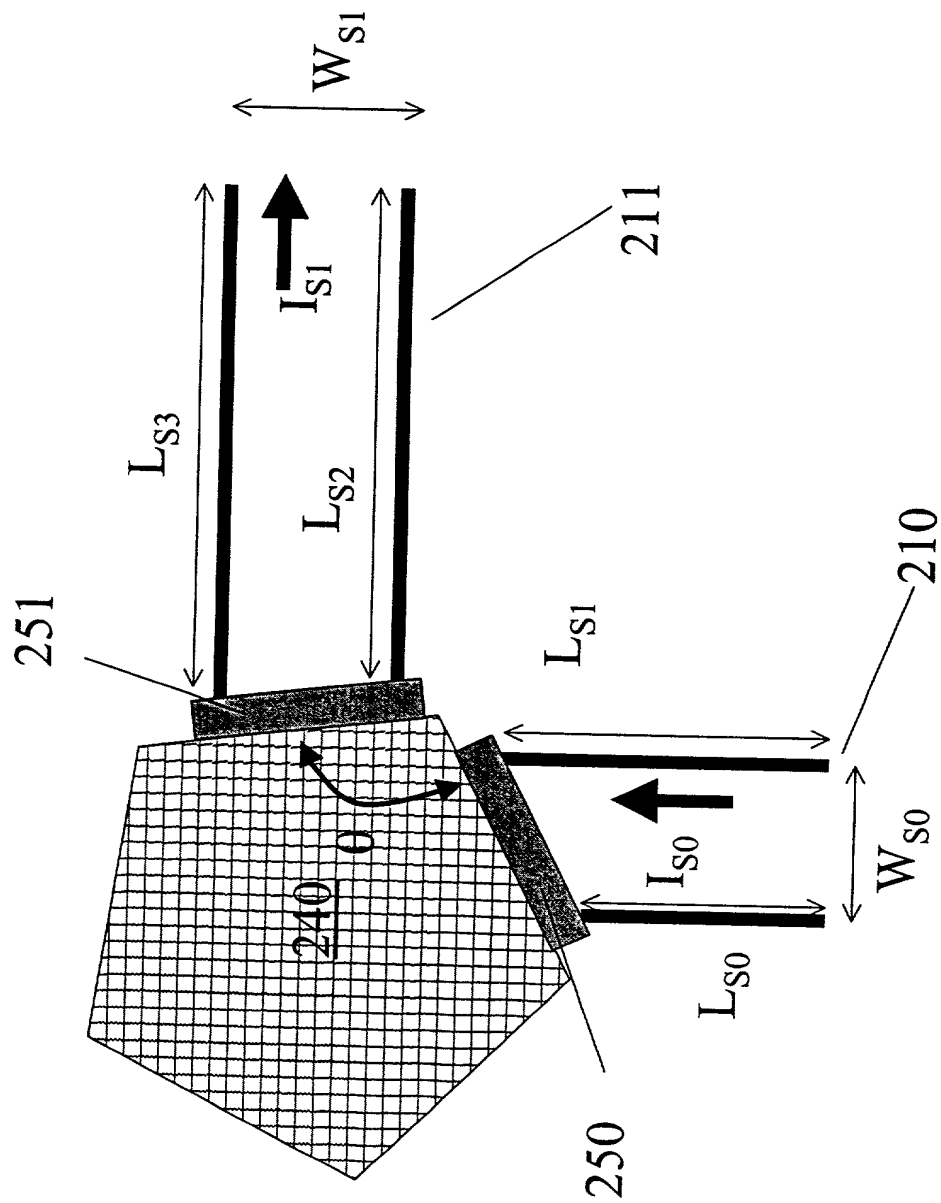






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Figure 2A



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FIG. 2B

Figure 2B

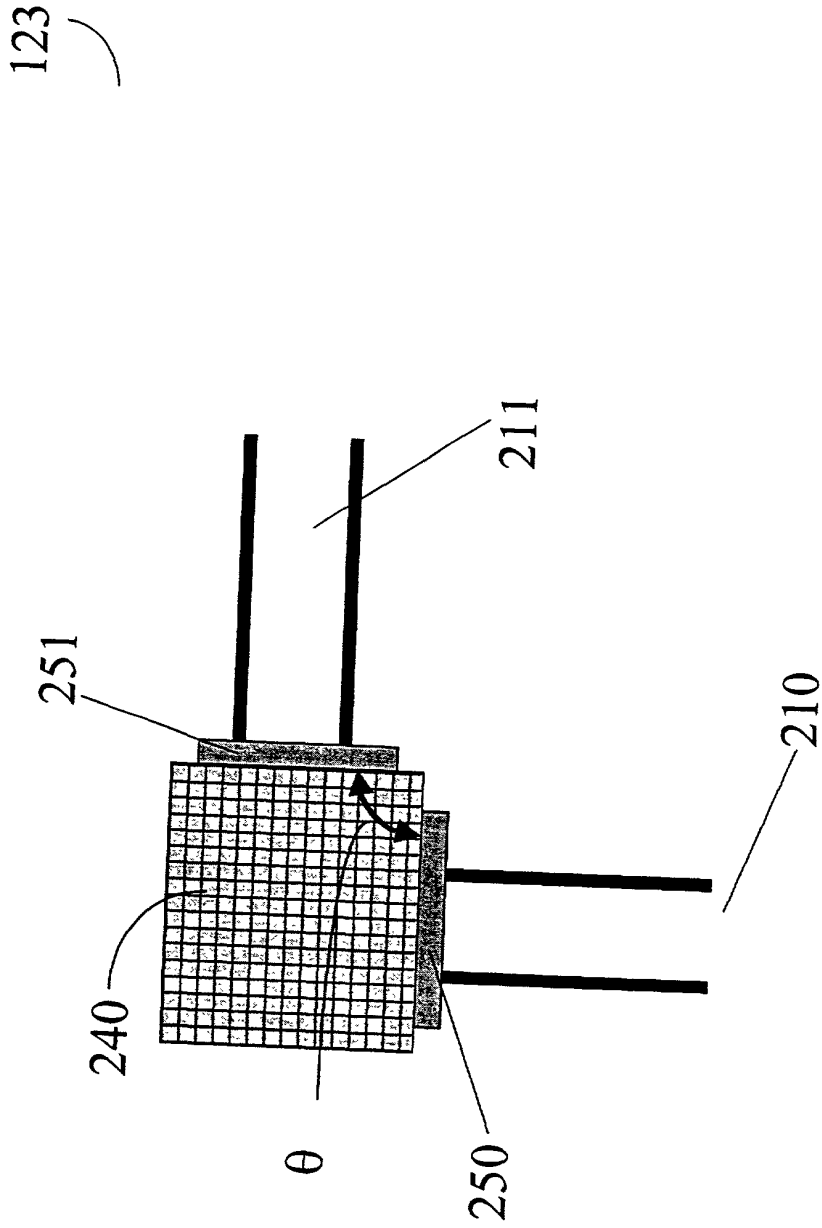


Figure 2C

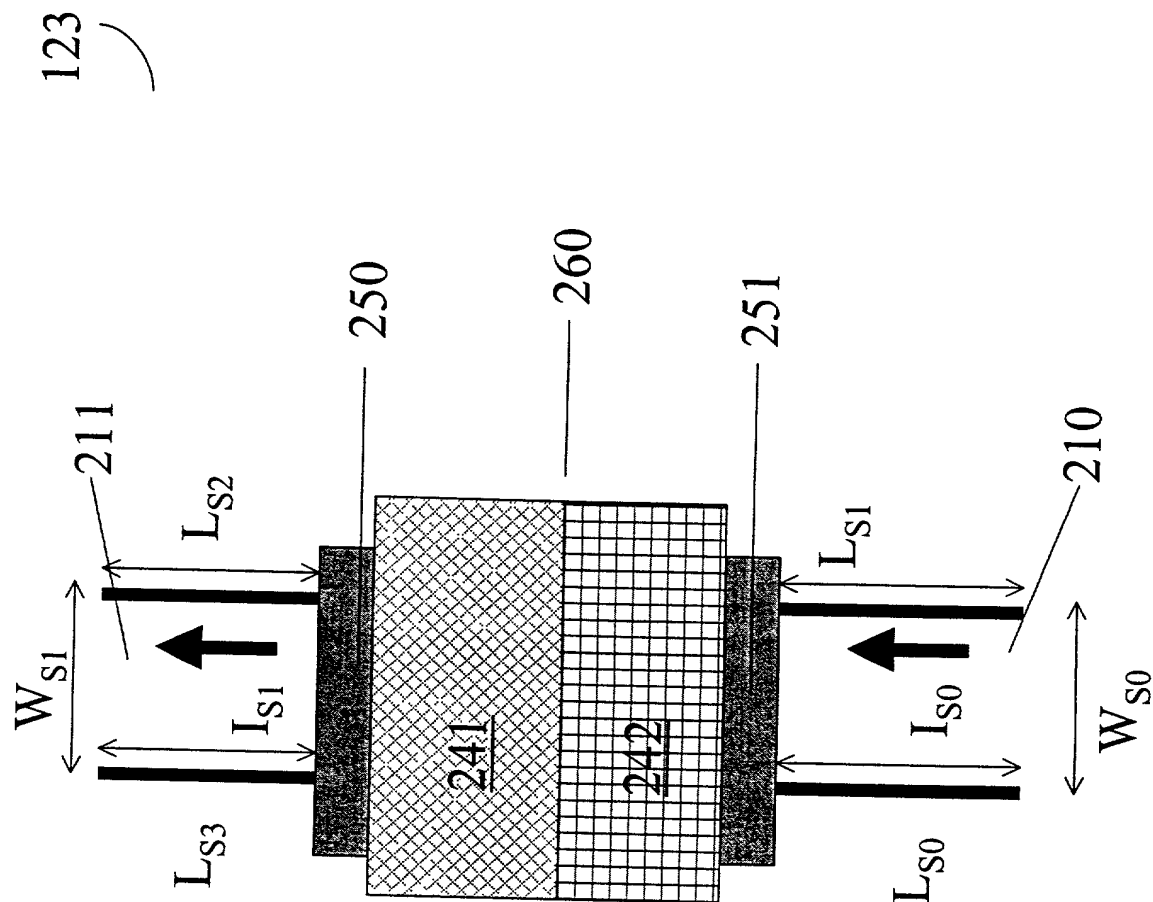


Figure 2D

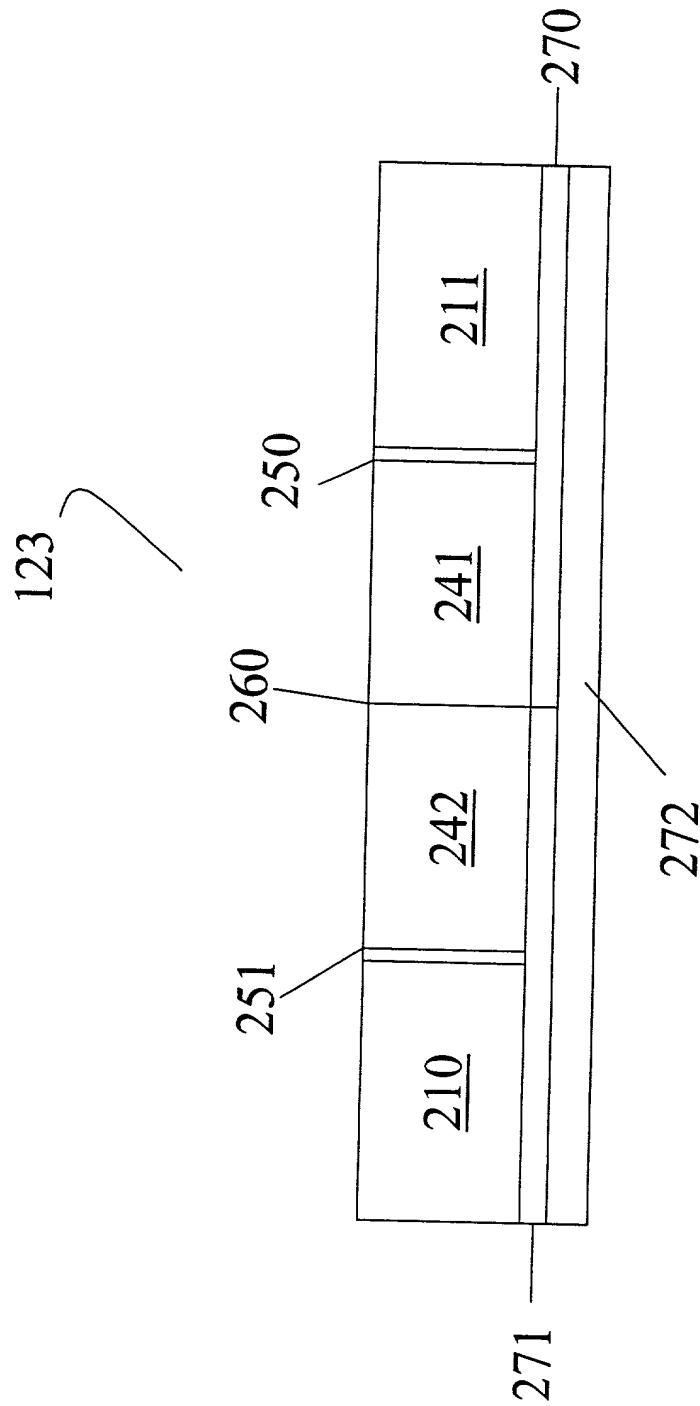


Figure 2E

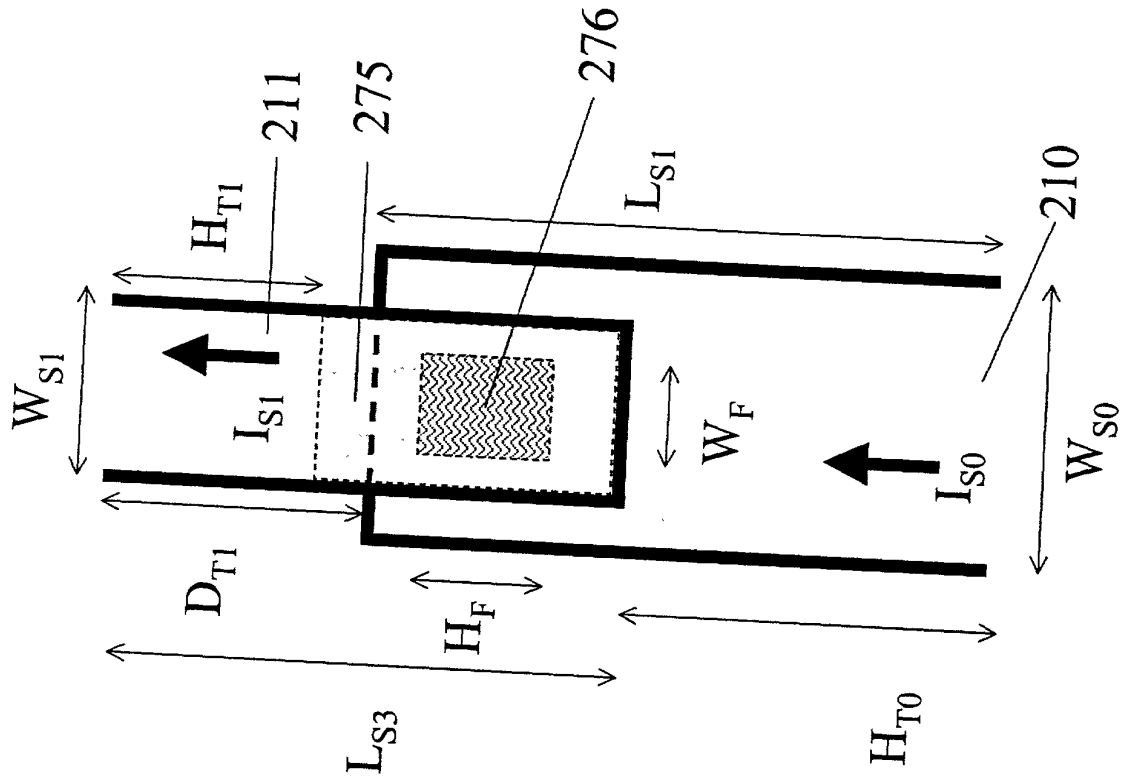
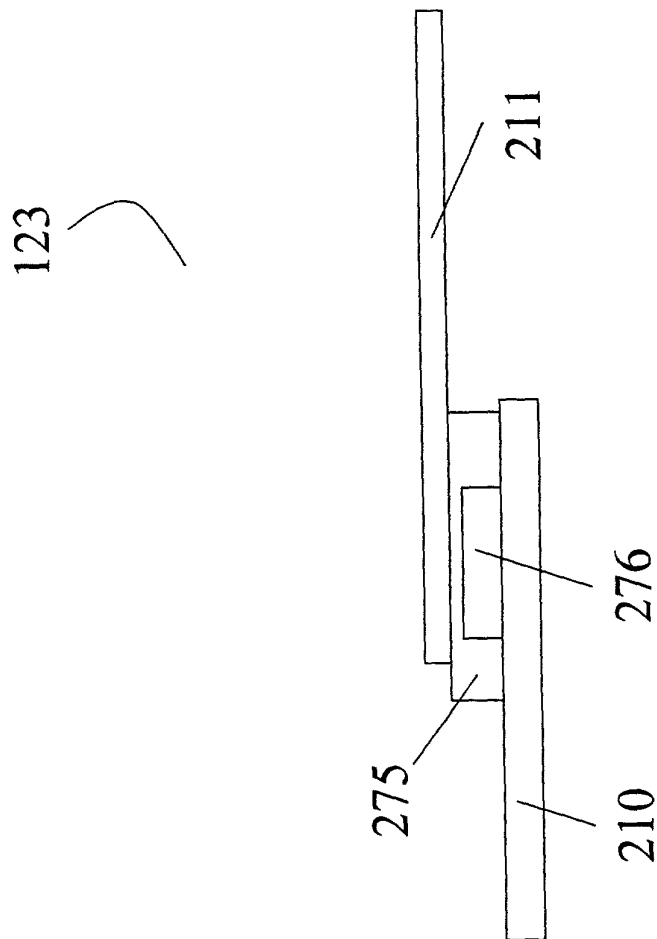


Figure 2F



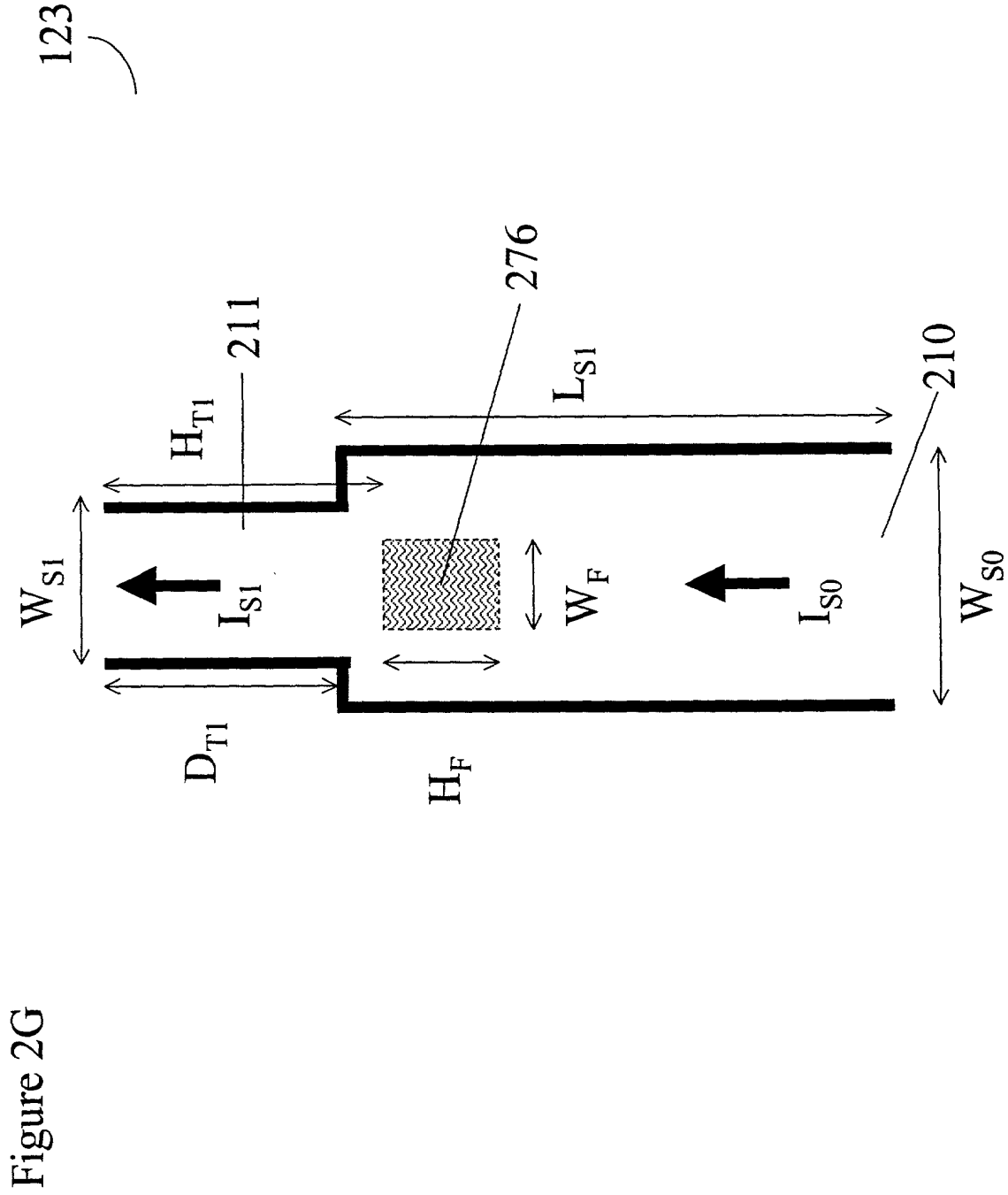


Figure 3A

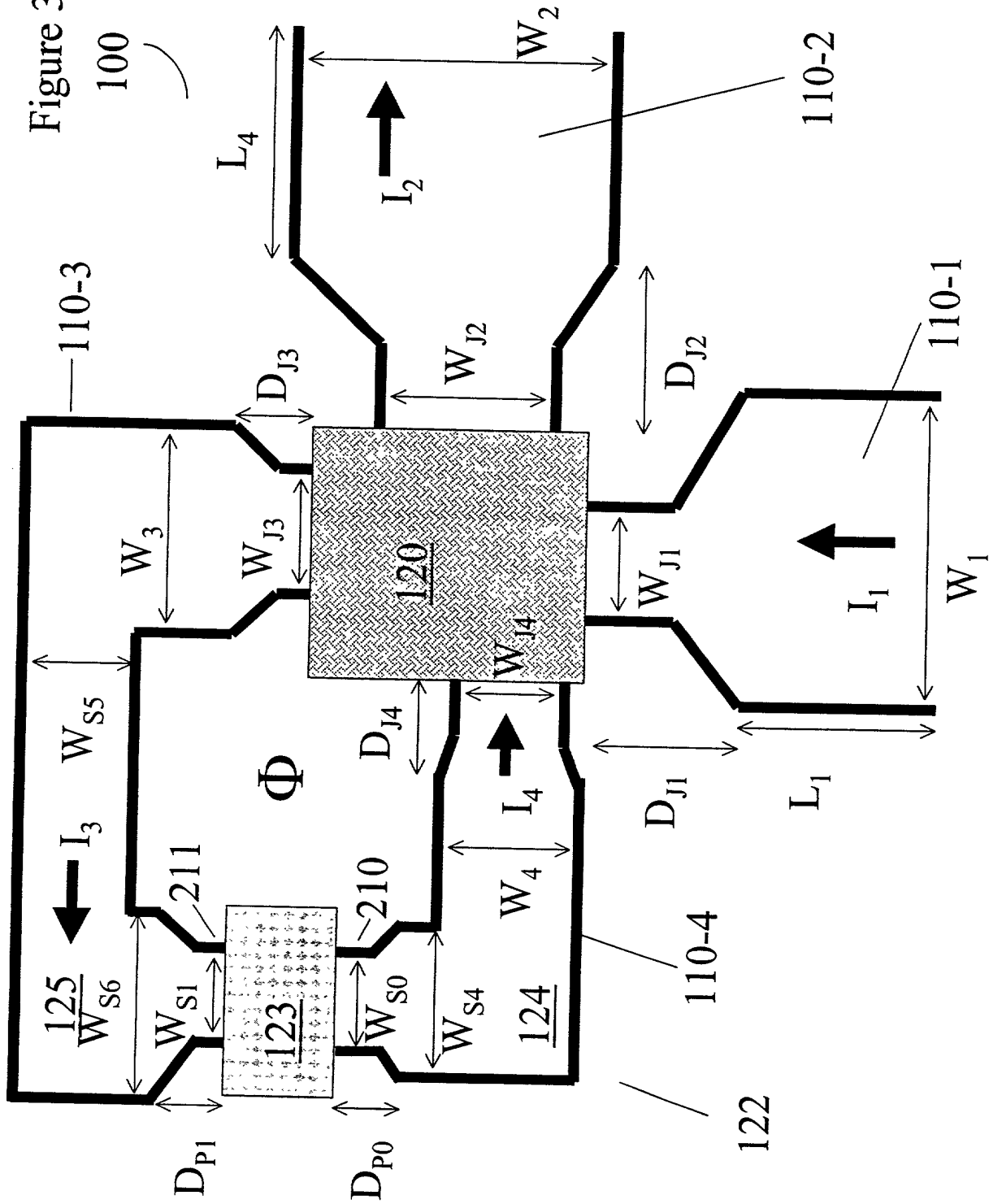


Figure 3B

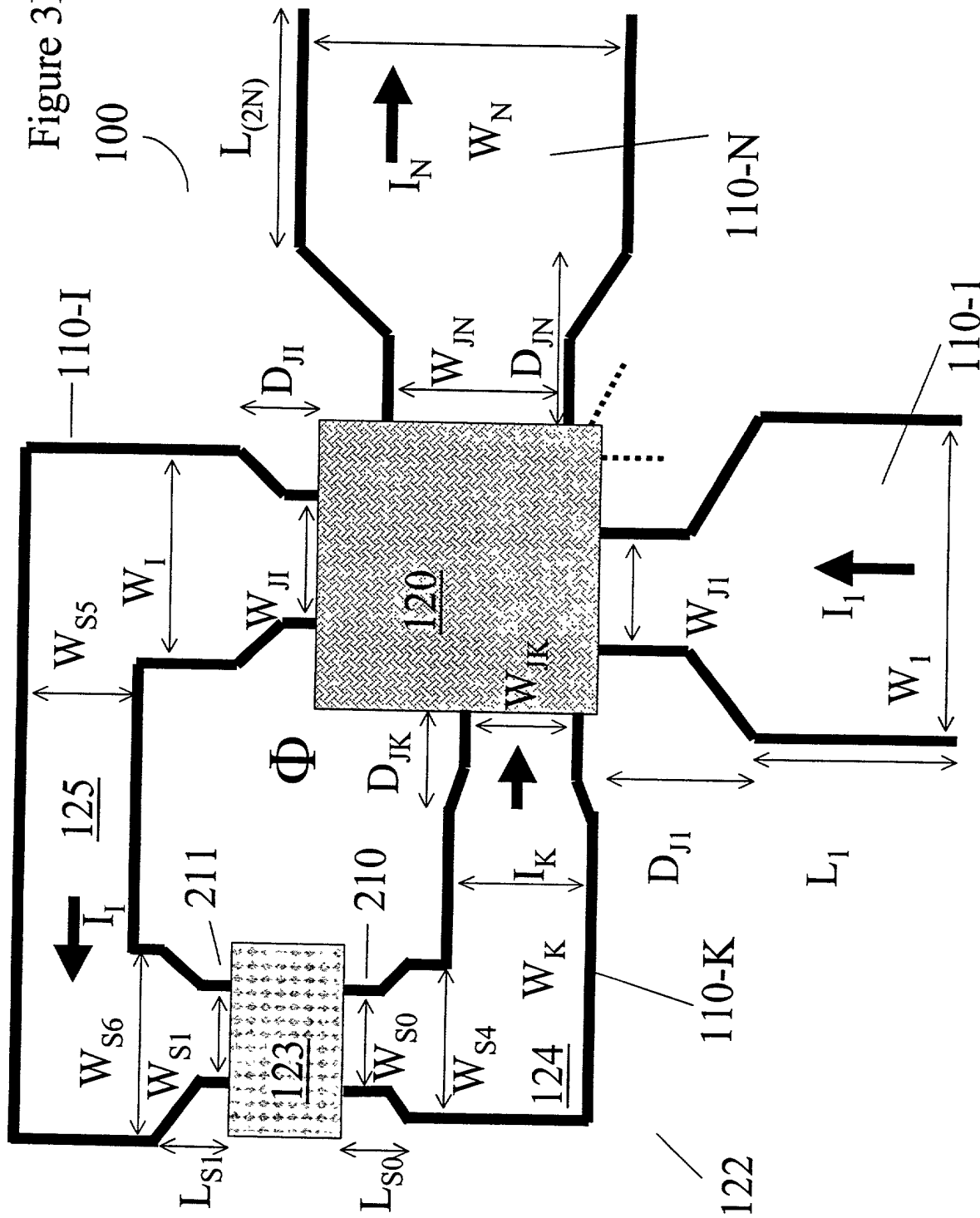
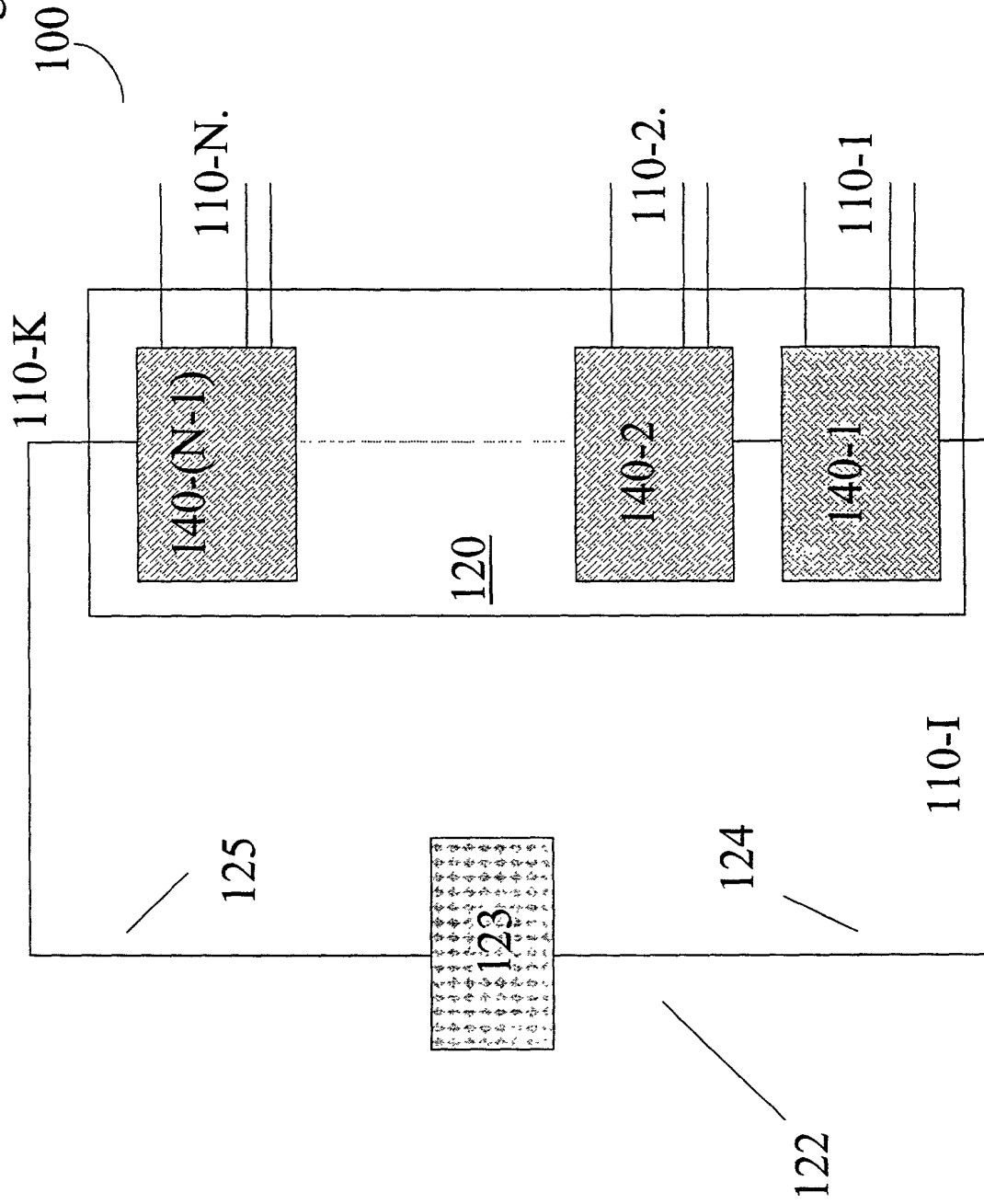


Figure 3C



The diagram illustrates a semiconductor device 400 with a series of gate structures. The device is divided into regions 410, 411, and 481. The gate structures are labeled 401-1, 401-2, ..., 401-N and 402-1, 402-2, ..., 402-N. Various dimensions are indicated, including W_{L1} , L_{L1} , W_{SL1} , W_{LN} , W_{L3} , W_{L2} , L_{L2} , W_{SL2} , W_{SL3} , L_{SL3} , and L_{SL2} . A current I_L is shown flowing to the right.

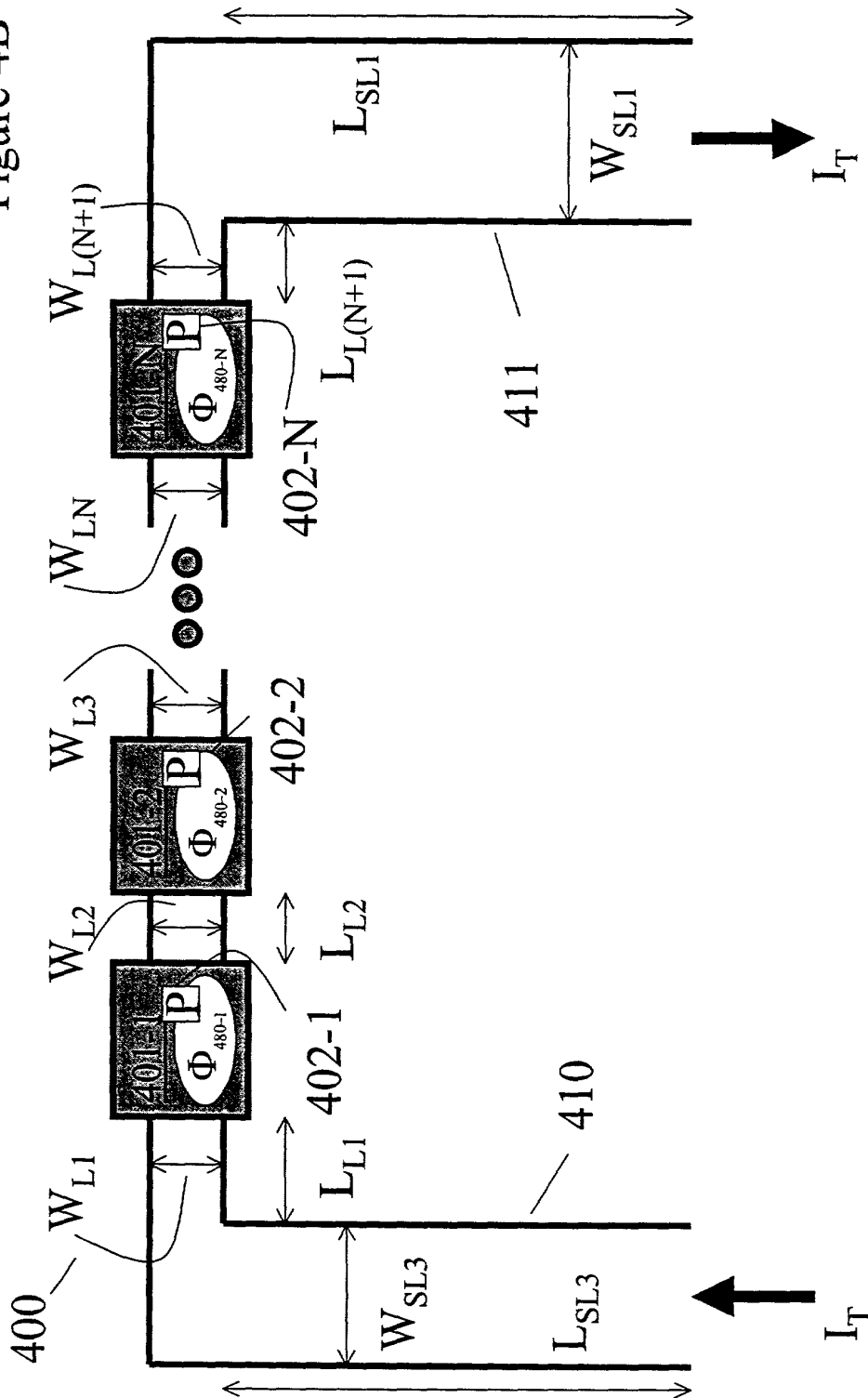
[illegible]

Figure 5

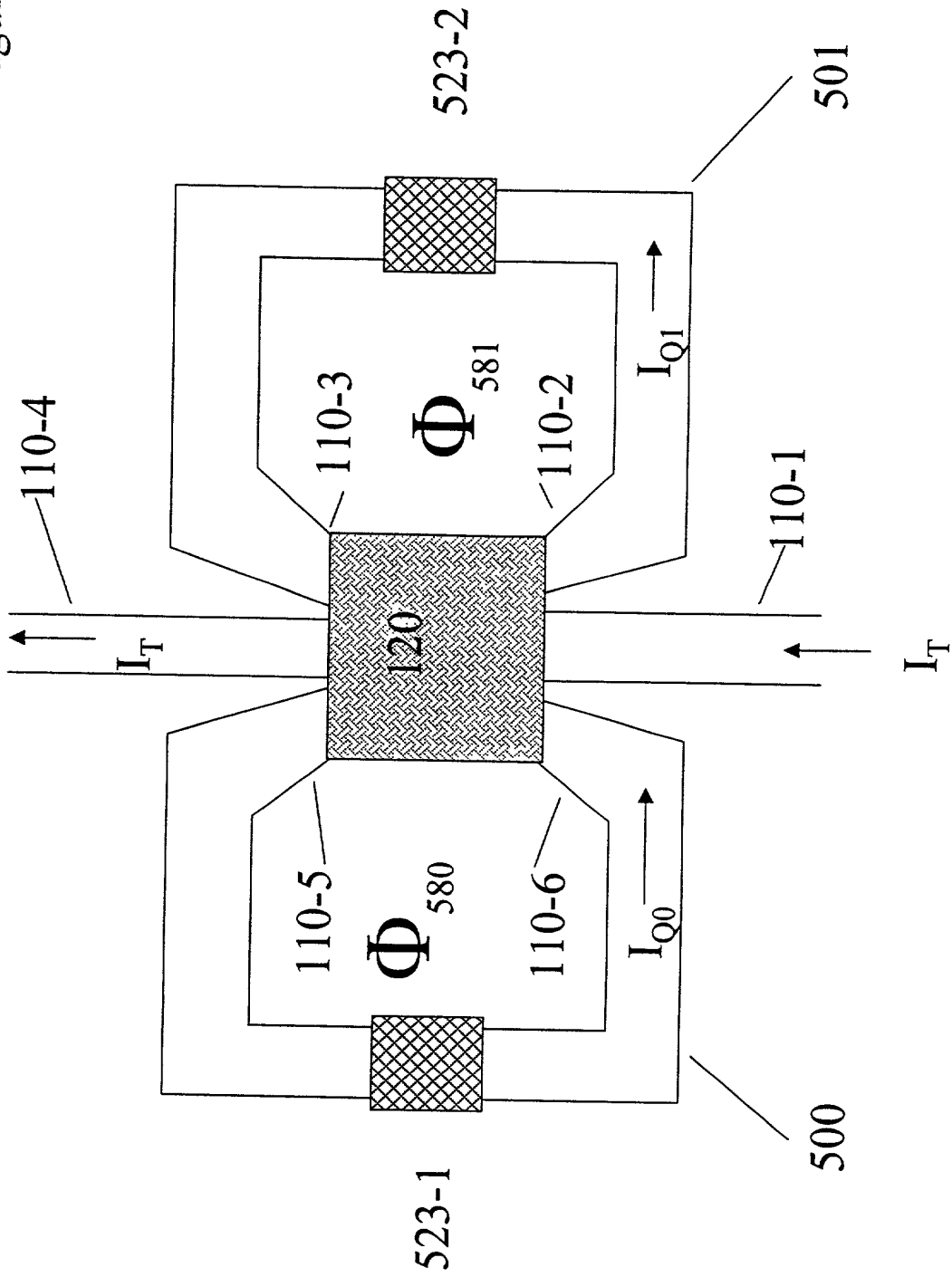


Figure 6A

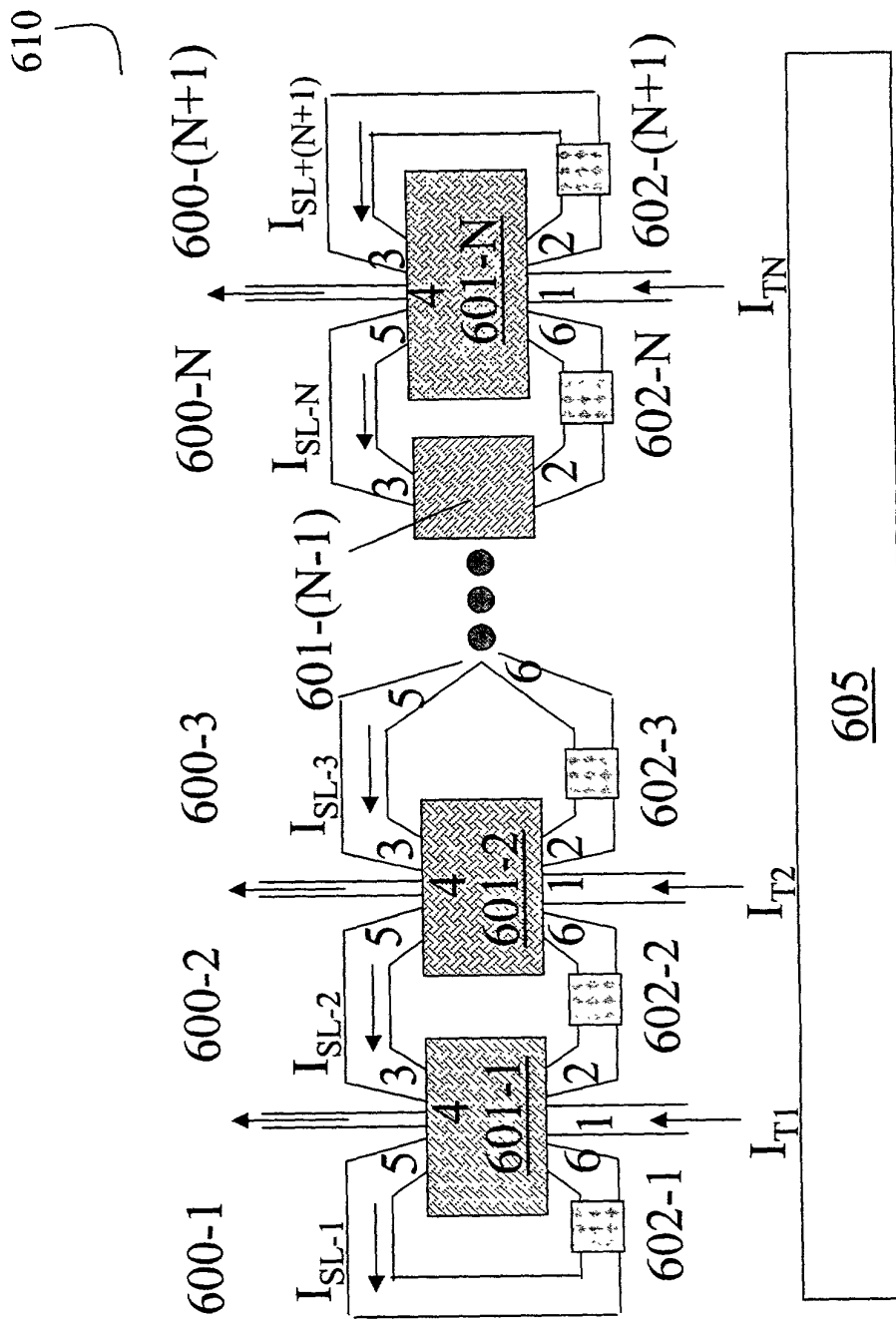


Figure 7

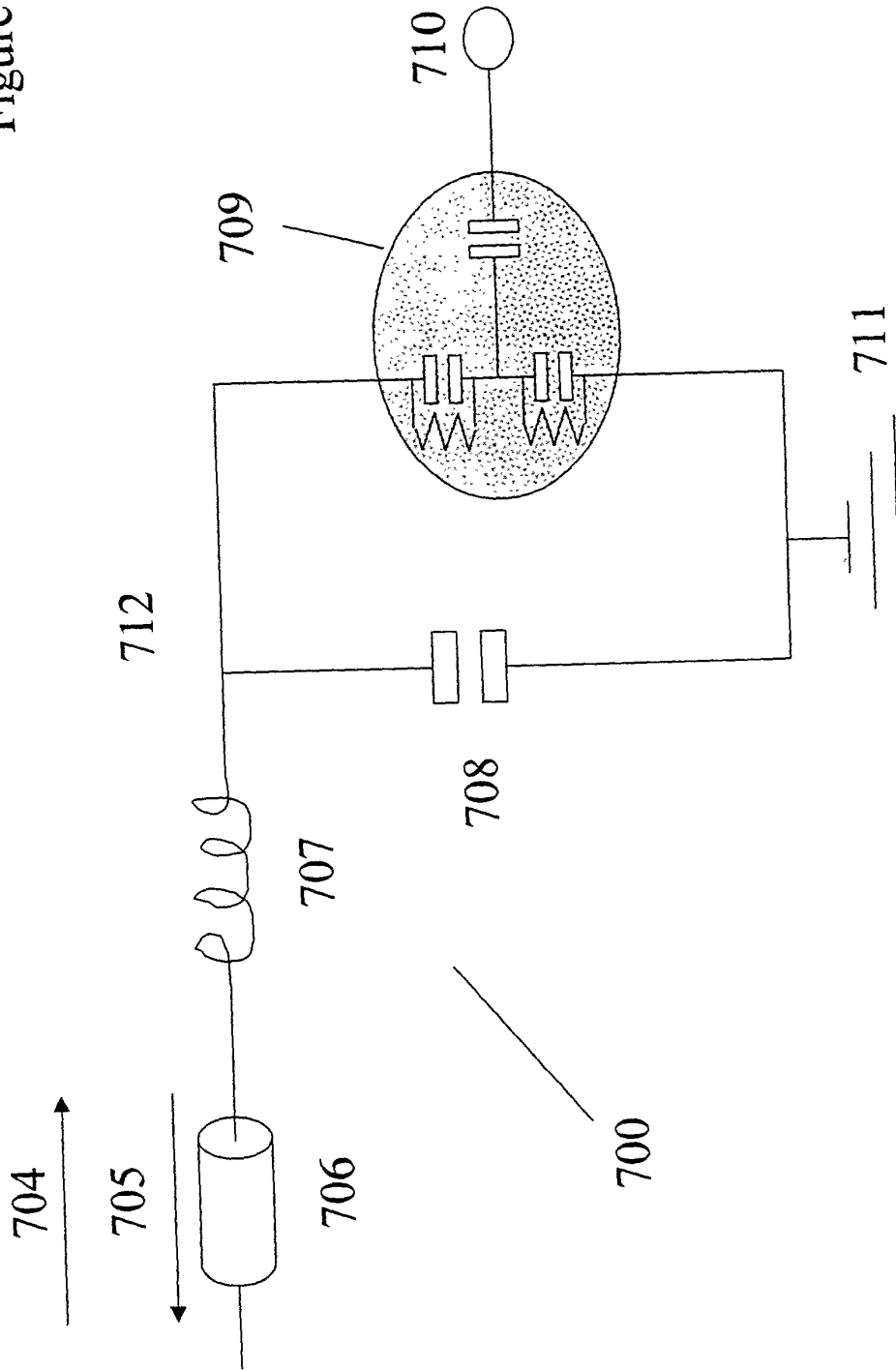


Figure 8

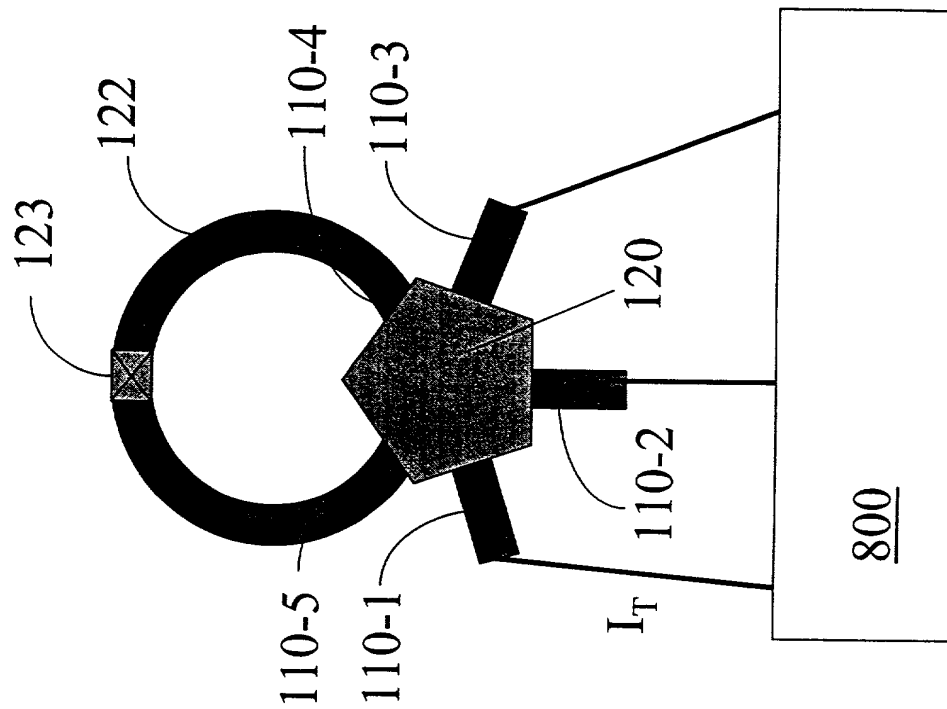
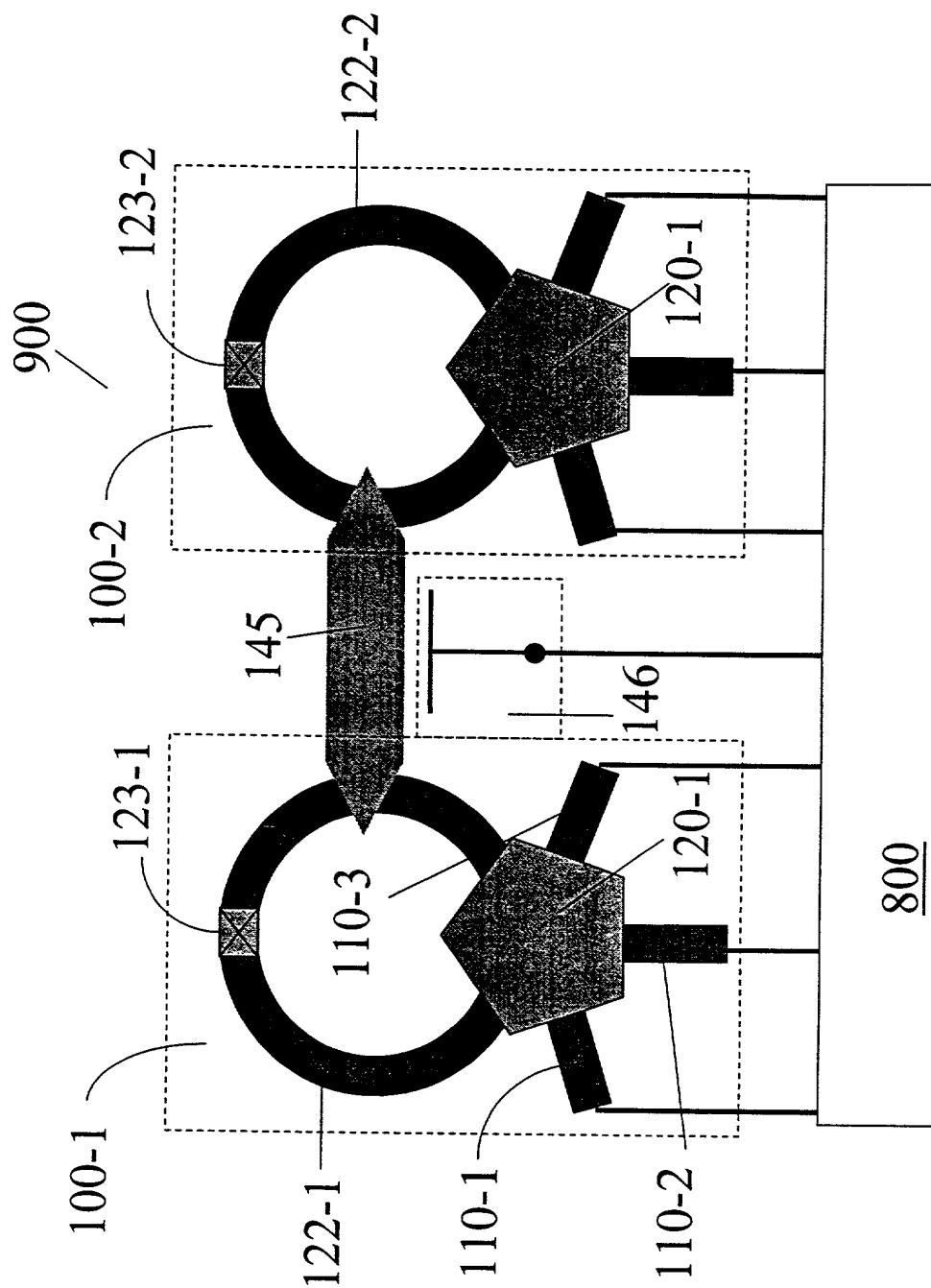


FIG. 8

Figure 9



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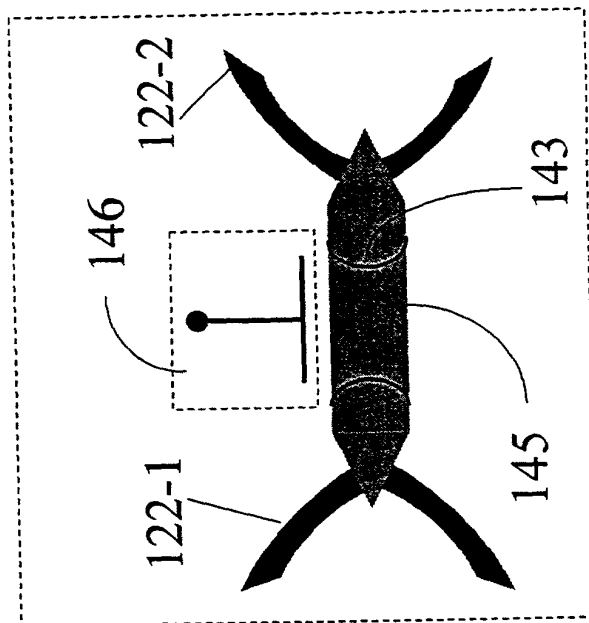


Figure 10a

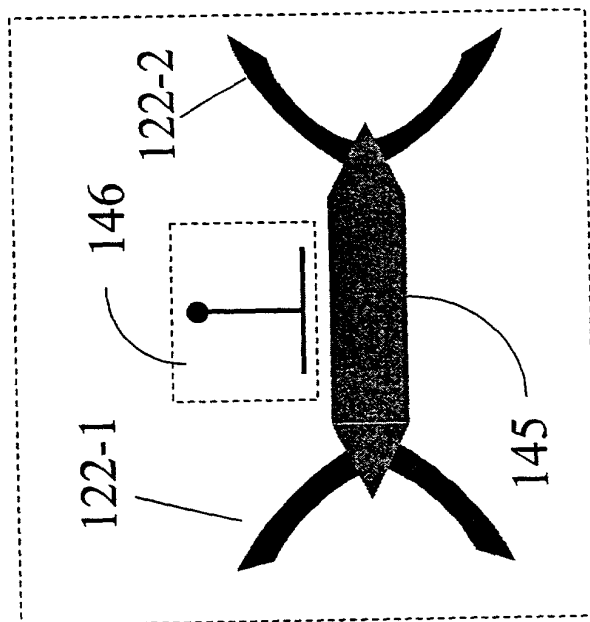


Figure 10b

FIG. 10a

Figure 11

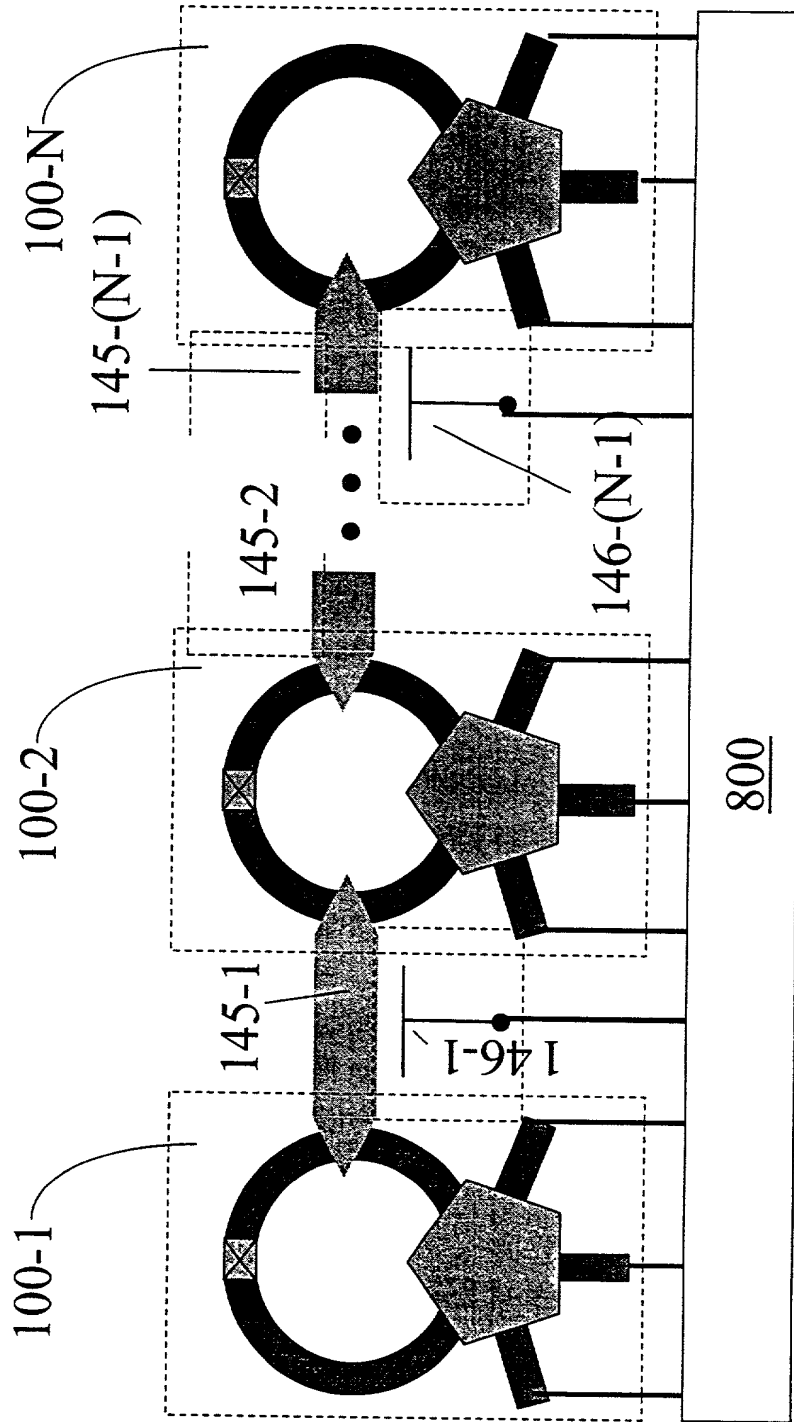
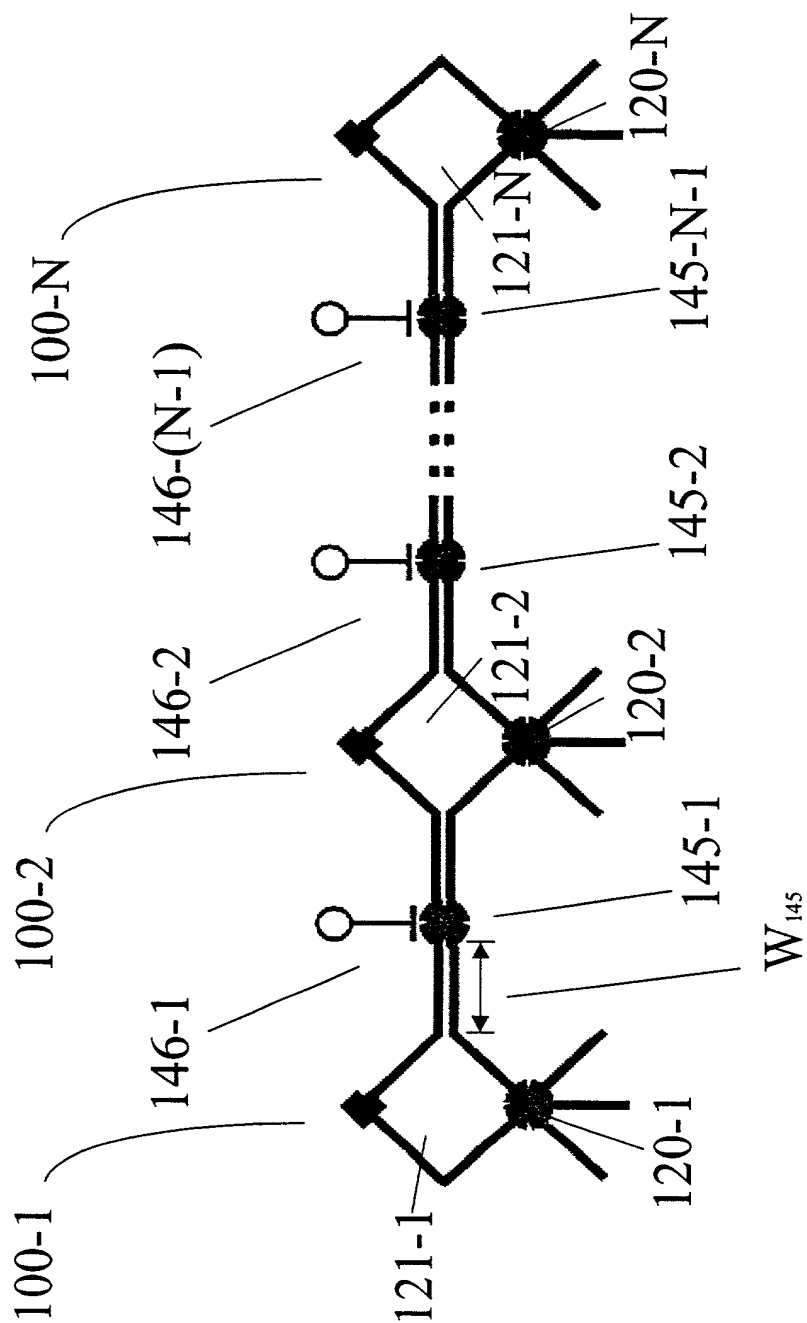
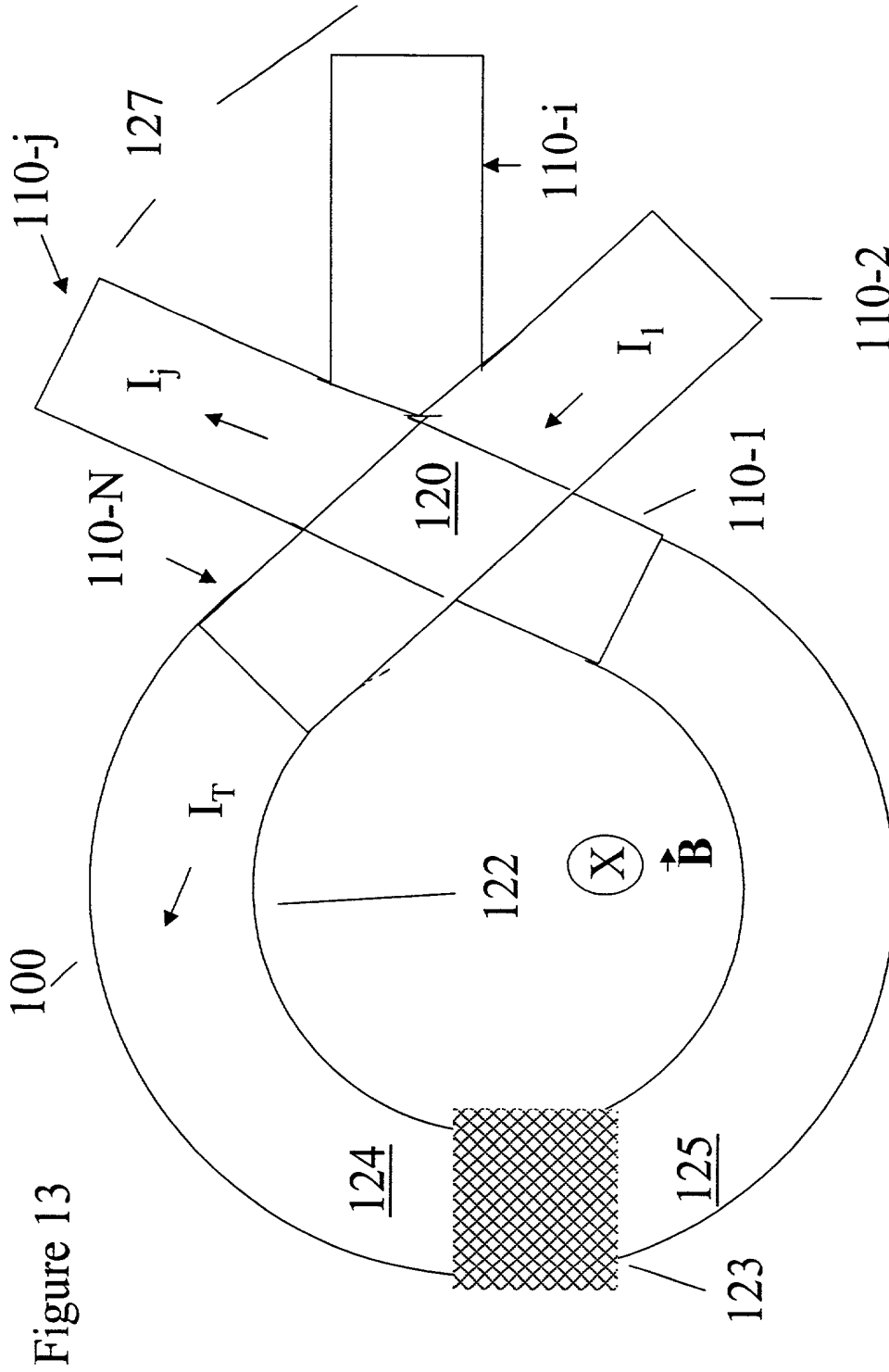


Figure 11

Figure 12





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